ABSTRACT

A channel architecture for use in automatic test equipment is disclosed. The channel architecture comprises pattern generation circuitry and timing circuitry responsive to the pattern generation circuitry to generate timing signals. Formatting circuitry coupled to the output of the timing circuitry generates pulse waveforms for application to pin electronics circuitry. The pin electronics circuitry is responsive to the formatting circuitry for interfacing the automatic test equipment to a device-under-test. The pattern generation circuitry, the timing circuitry, the formatting circuitry and the pin electronics circuitry are formed on the same integrated circuit.